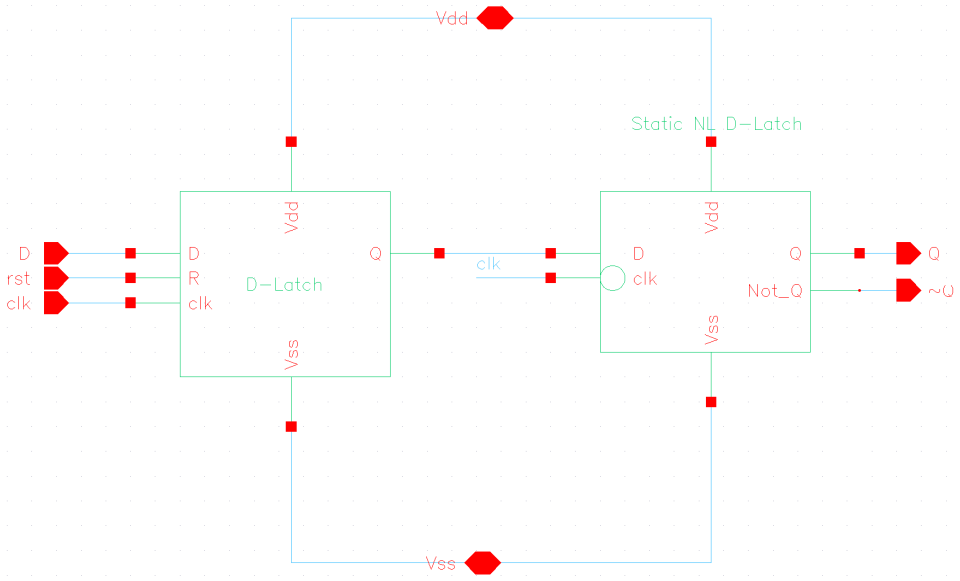
ELE 448 Lab 6

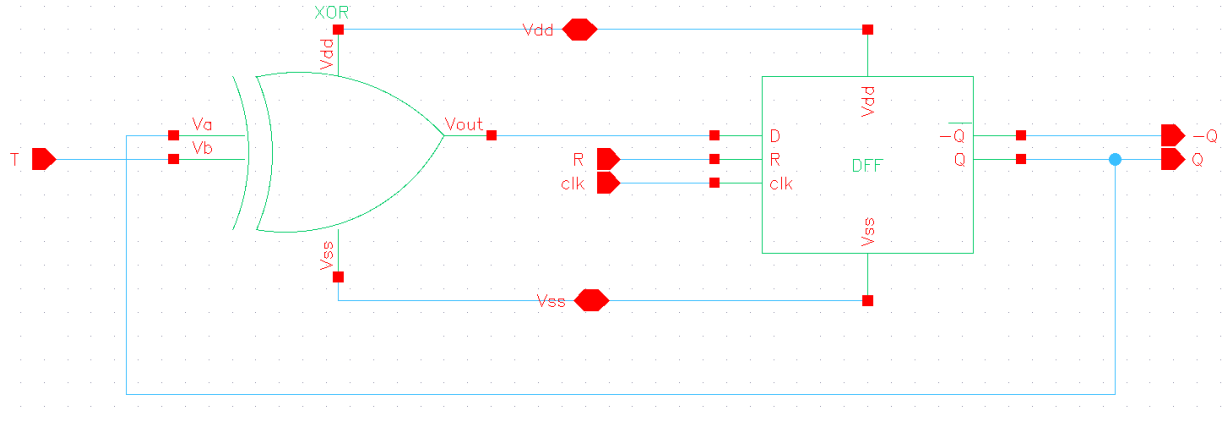
Due by 1 April, 2020 (estimated)

Introduction:

A flip-flop differs from a latch due to the fact that its output is updated on the edge of a clock signal rather than its logic level. To realize a flip-flop, two latches need to be cascaded together as seen in following schematic.

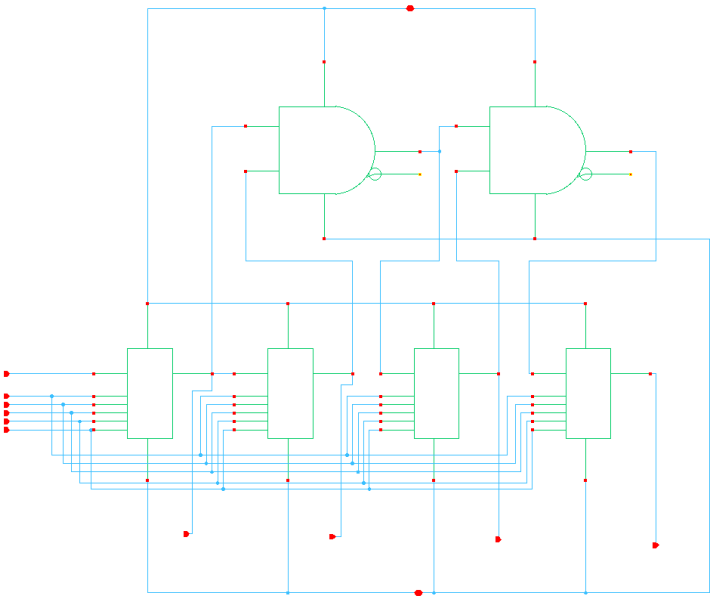


A Toggle Flip-Flop, or T Flip-Flop (TFF) is used to toggle the output when the input is high (1.8V). This is accomplished by using a XOR and D Flip-Flop (DFF) as seen by the schematic below:



As expected, the output will not update instantaneously when T is high. The DFF will only pass the toggle signal on a clock edge when reset is high. Using a negative edge DFF, changes will be passed to the output on a negative edge of the clock.

An application for the TFF is a binary counter. This is apparent from the fact that when T is connected to a voltage corresponding to a logic high, the output will alternate between a 0 and a 1 every clock cycle. In order to achieve N-bit counters, N TFFs need to be cascaded together. For a counter to work, the frequency at which each stage toggles needs to be half the frequency of the previous stage. This can be done by using the output of the first TFF as the input to the second TFF; however, all other stages should only be high when all previous stages are high. This means that for an N-bit counter, N-2 AND gates are needed. A 4-bit counter can be seen below:



Assignments:

1. Negative Edge D Flip-Flop
    a. Open the schematic editor; wire the Negative Edge D Flip-Flop as shown in the introduction
        i. How many transistors are required for this design?
    b. Create a symbol
    c. Verify the schematic (make sure simulations yield useful information)
    d. Generate the layout; verify the layout, e.g. DRC & LVS

2. TFF
    a. Open the schematic editor; wire the T Flip-Flop as shown in the introduction
        i. How many transistors are required for this design?
    b. Create a symbol
    c. Verify the schematic
        i. How does the TFF operate?
        ii. What does its truth table look like?

3. Load the primitiveCells library into your workspace
    a. Open the command terminal on the lynx machine
    b. Type: cp -a /u/ugrads/tmauldin/Public/primitiveCells/ /u/ugrads/<username>/<directory_name>/
        i. Don't include "<>" in the path
    c. Start Cadence (IC615) from your directory
    d. Create a new library with the following properties
        i. Name: primitiveCells (case sensitive)
        ii. Path: /u/ugrads/<your_username>/<your_directory_name>
        iii. Attach to TSMC 0.2u CMOS018

    Note:

    - The cells in this library should be used for all designs created throughout the remainder of this semester

4. 4-Bit Counter
    a. Create a schematic
        i. This will be completed using the TFF and AND cells
    b. Create a symbol
    c. Test the performance
        i. In order to test the counter, a two phase clock is required with two inverters

    Questions:

    - What TFF represents the LSB and which one represents the MSB?
    - What is the count sequence?
    - How many clock cycles are required to count from 0 to 15?